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-	2	("6166961").PN.	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/02 12:41
-	11614	negative near10 pump\$1	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/02 12:49
-	12869	eras\$3 near5 (voltage\$1 or potential)	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/02 12:49
-	53321	read\$3 near5 (voltage\$1 or potential)	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/02 12:49
-	345	((negative near10 pump\$1) and (eras\$3 near5 (voltage\$1 or potential)) and (read\$3 near5 (voltage\$1 or potential)))	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/02 12:49
-	449909	driver\$1	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/02 12:52
-	73808	365/\$7	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/02 12:54
-	140	((negative near10 pump\$1) and (eras\$3 near5 (voltage\$1 or potential)) and (read\$3 near5 (voltage\$1 or potential))) and driver\$1 and 365/\$7	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/02 12:54
-	7168	level adj shifter\$1	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/08 09:45
-	2623	negative adj3 pump\$1	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/08 09:47
-	12772	positive adj3 pump\$1	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/08 09:50
-	249554	(block\$1 or bank\$1) near5 control\$4	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/08 10:22
-	73956	365,\$7	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/08 10:25
-	2	(level adj shifter\$1) and (negative adj3 pump\$1) and (positive adj3 pump\$1) and ((block\$1 or bank\$1) near5 control\$4) and 365,\$7	USPAT; US-PGPUB; EPO; JPO; DEFWENT; IBM_TLB	2003/07/08 10:25



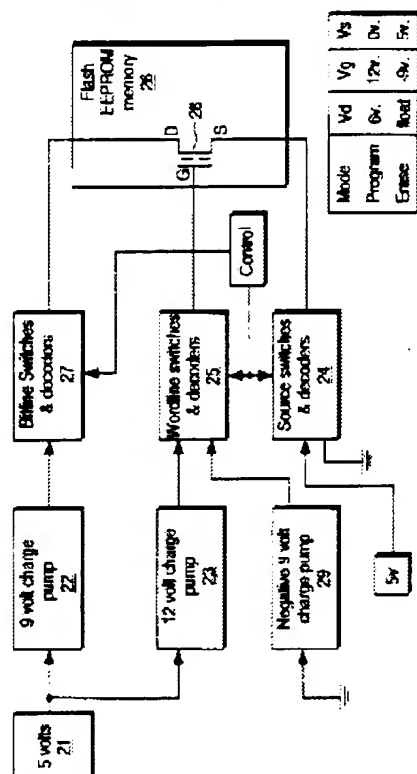
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FIG. 2



(12) **United States Patent**
Rao(03) Patent No.: **US 6,359,947 B1**
(45) Date of Patent: **Mar. 19, 2002**(54) **SPLIT CLOCK BUFFERS FOR A NEGATIVE CHARGE PUMP**(75) Inventor: **Hari M. Rao, Fair Oaks, CA (US)**(73) Assignee: **Intel Corporation, Santa Clara, CA (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days

(21) Appl. No.: **09/387,641**(22) Filed: **Aug. 31, 1999**(51) Int. Cl.⁷: **H03D 3/24**(52) U.S. Cl.: **375/374, 327/536**(58) Field of Search: **375/374, 327/536, 327/530, 306; 365/226, 215, 149****References Cited****U.S. PATENT DOCUMENTS**

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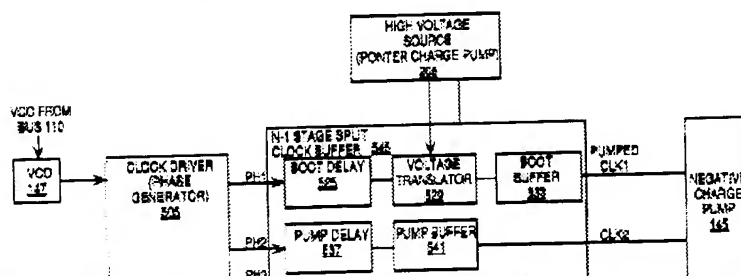
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ABSTRACT

A split clock buffer for providing clock signals to a negative charge pump. The split clock buffer receives a first phase and a second phase of the clock signal, pumps the voltage level of the first phase from a first voltage level to a second voltage level. Then, the buffer outputs the pumped first phase to a boot node of the negative charge pump, and outputs the second phase to a pump node of the negative charge pump.

37 Claims, 12 Drawing Sheets

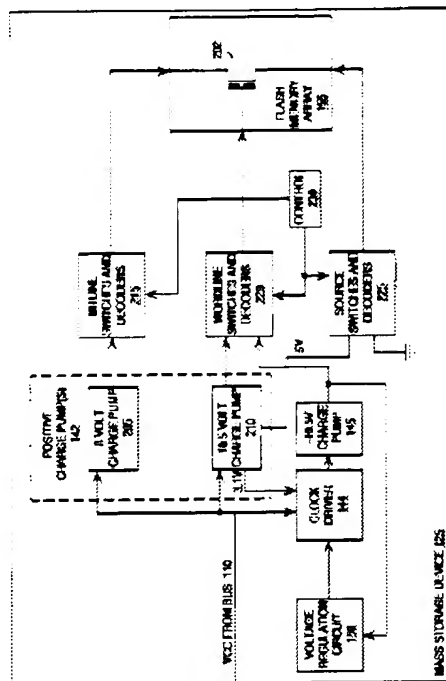
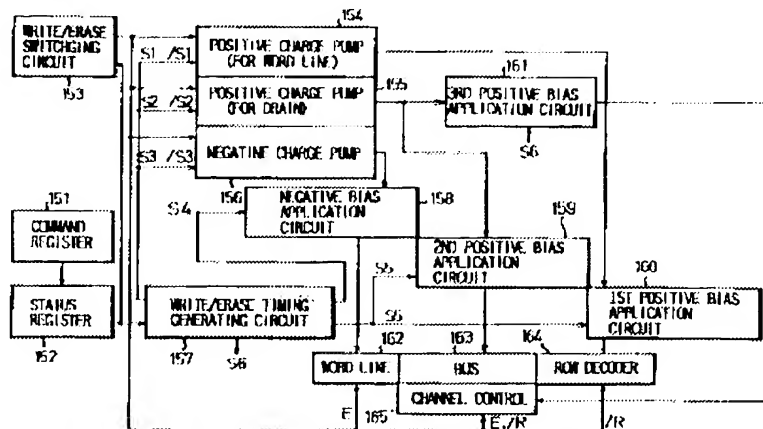


FIG. 2

Fig.9



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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Ret
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2	<input type="checkbox"/>	<input type="checkbox"/>	US 6278327 B1	20010821	6	Negative voltage detector	330/297	257/227; 330/279	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6160440 A	20001212	14	Scaleable charge pump for use with a low voltage power	327/536	327/589; 363/60	
4	<input type="checkbox"/>	<input type="checkbox"/>	US 5973979 A	19991026	11	Low supply voltage negative charge pump	365/226	365/185.33; 365/218	
5	<input type="checkbox"/>	<input type="checkbox"/>	US 5774411 A	19980630	18	Methods to enhance SOI SRAM cell stability	365/230.06	365/156; 365/204	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 5692164 A	19971125	13	Method and apparatus for generating four phase	713/501	327/296; 327/536	
7	<input type="checkbox"/>	<input type="checkbox"/>	US 5581107 A	19961203	42	Nonvolatile semiconductor memory that eases the	257/392	257/322; 257/348;	
8	<input type="checkbox"/>	<input type="checkbox"/>	US 5553295 A	19960903	10	Method and apparatus for regulating the output	713/300	363/60; 365/218;	
9	<input type="checkbox"/>	<input type="checkbox"/>	US 5532915 A	19960702	12	Method and apparatus for providing an ultra low power	363/60	327/536	
10	<input type="checkbox"/>	<input type="checkbox"/>	US 5406524 A	19950411	41	Nonvolatile semiconductor memory that eases the	365/185.27	365/185.1; 365/185.18;	

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